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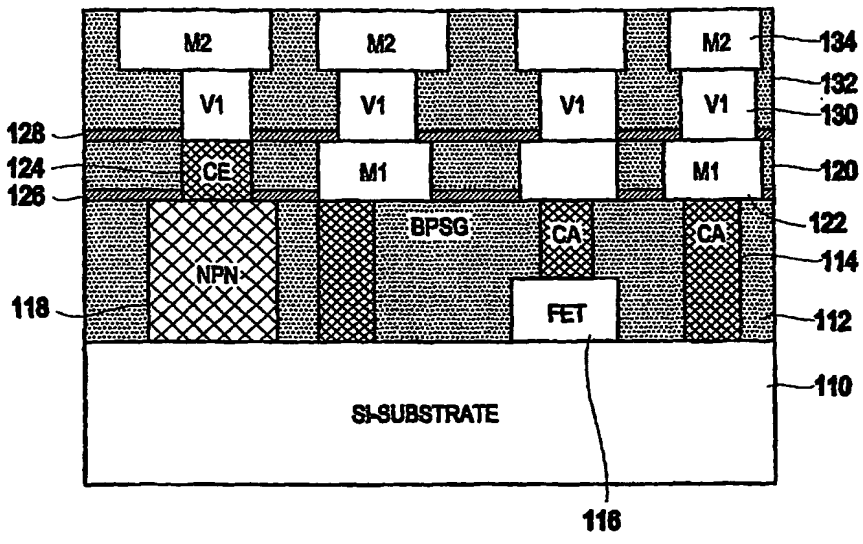
(54) Title: BIPOLAR AND CMOS INTEGRATION WITH REDUCED CONTACT HEIGHT



(57) Abstract: Disclosed is a method and structure for an integrated circuit structure that includes a plurality of complementary metal oxide semiconductor (CMOS) transistors (116) and a plurality of vertical bipolar transistors (118) positioned on a single substrate (110). The vertical bipolar transistors (118) are taller devices than the CMOS transistors (116). In this structure, a passivating layer (112) is positioned above the substrate (110), and between the vertical bipolar transistors (118) and the CMOS transistors (116). A wiring layer (120) is above the passivating layer (112). The vertical bipolar transistors (118) are in direct contact with the wiring layer (120) and the CMOS transistors (116) are connected to the wiring layer (114) by contacts extending through the passivating layer (112).

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